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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,973	03/24/2004	Christopher Joseph Michalski	55123P271	4464

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,973	MICHALSKI, CHRISTOPHER JOSEPH	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-13 and 21-26* is/are allowed.

6)☒ Claim(s) *1-6 and 14-19* is/are rejected.

7)☒ Claim(s) *7 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/02/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 14-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Randazzo et al (U.S Patent No. 6,803,801).

Randazzo et al disclose in Figs. 7-9 a level shifter circuit including:

Regarding claim 1:

a first NMOS device (48) having a source, a drain and a gate;

a second NMOS device (44) having a source, a drain and a gate;

the source of the second NMOS device (44) being connected to the drain of the first NMOS device (48);

the gate of the first (48) and second (44) NMOS devices being coupled together;

the gate of the first NMOS device (48) being coupled to the gate connection, the drain of the second NMOS device (44) being coupled to the drain connection and the source of the first transistor (48) being coupled to the source connection;

the second NMOS device (44) having a lower threshold voltage than the first NMOS transistor (48) (NMOS 44 has a nearly zero threshold voltage, see col. 3, line 18).

Regarding the limitation of claim 2: because the claimed structure is fully met by Randazzo, the recited function recited therein will necessarily be inherent in Randazzo, as held by the court in In re Best, 195 USPQ 430.

Regarding claim 3: the second NMOS device is a native device (44).

Regarding claim 4: the second NMOS has a substantially zero threshold (see col. 3, line 18).

Regarding claim 5: the gates of the first (48) and second (44) NMOS devices are coupled together through a bias control (VDD12).

Regarding claim 6: the bias control compensates for variations in temperature and processing is inherent seen in col. 1, lines 49-50 and col. 2, lines 8-10.

Regarding claim 14:

a first NMOS device (48) having a source, a drain and a gate;

a second NMOS device (44) having a source, a drain and a gate;

a current source (is seen as 46);

the source of the second NMOS device (44) being connected to the drain of the first NMOS device (48);

the gates of the first (48) and second (44) NMOS devices being coupled together;

the gate of the first NMOS device (48) being coupled to the source follower input connection (VDD12), the drain of the second NMOS device (44) being coupled to the positive power supply connection (VDDIO33) and the source of the first transistor (48) being coupled to the source follower output connection (connection between 48 and 46) and through the current source (46) to the circuit ground connection (seen as VSSIO, see Fig. 8);

the second NMOS device (44) having a lower threshold voltage than the first NMOS transistor (48) (NMOS 44 has a nearly zero threshold voltage, see col. 3, line 18).

Claim 15 is similarly rejected as claim 2.

Claim 16 is similarly rejected as claim 3.

Claim 17 is similarly rejected as claim 4.

Claim 18 is similarly rejected as claim 5.

Claim 19 is similarly rejected as claim 6.

Allowable Subject Matter

Claims 7 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "the bias control is coupled to the gate of the second NMOS through a resistor, and wherein the gates of the first and second NMOS devices are AC coupled together" as recited in claims 7 and 20.

Claims 8-13 and 21-26 are allowable over the prior art of record. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "the gate of the second NMOS device being coupled to the source of the first NMOS device" in combination with "the source of the second NMOS device being connected to the drain of the first NMOS device" as recited in claims 8 and 21.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

March 10, 2005